

SWITCHING

DUAL P-CHANNEL POWER MOS FET

INDUSTRIAL USE

DESCRIPTION

The μ PA1770 is a P-channel MOS Field Effect Transistor designed for power management applications of portable machines.

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1770G	Power SOP8

FEATURES

- Dual chip type
- Low on-resistance
 $R_{DS(on)1} = 37 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.5 \text{ V, } I_D = -3.0 \text{ A)}$
 $R_{DS(on)2} = 39 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.0 \text{ V, } I_D = -3.0 \text{ A)}$
 $R_{DS(on)3} = 59 \text{ m}\Omega \text{ MAX. (} V_{GS} = -2.5 \text{ V, } I_D = -3.0 \text{ A)}$
- Low input capacitance
 $C_{iss} = 1300 \text{ pF TYP.}$
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, All terminals are connected.)

Drain to Source Voltage	V_{DSS}	-20	V
Gate to Source Voltage	V_{GSS}	∓ 12	V
Drain Current (DC)	$I_{D(DC)}$	∓ 6.0	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	∓ 24	A
Total Power Dissipation (1 unit) ^{Note2}	P_T	0.40	W
Total Power Dissipation (2 unit) ^{Note2}	P_T	0.75	W
★ Total Power Dissipation (1 unit) ^{Note3}	P_T	1.7	W
★ Total Power Dissipation (2 unit) ^{Note3}	P_T	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Mounted on FR4 Board of $1600 \text{ mm}^2 \times 1.6 \text{ mm}$, Drain Pad size : $4.5 \text{ mm}^2 \times 35 \mu\text{m}$, $T_A = 25^\circ\text{C}$

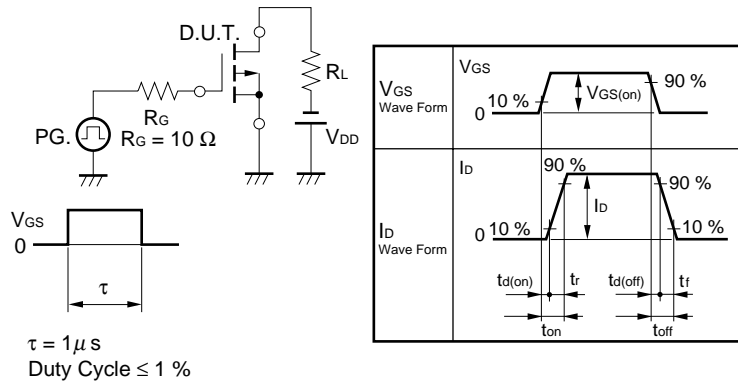
★ **3.** Mounted on ceramic substrate of $1200 \text{ mm}^2 \times 2.2 \text{ mm}$, $T_A = 25^\circ\text{C}$

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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

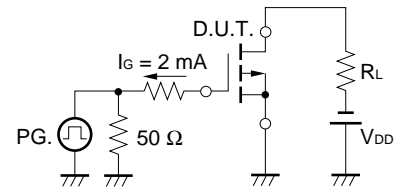
★ ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = -4.5 V, I _D = -3.0 A		28	37	mΩ
	R _{DS(on)2}	V _{GS} = -4.0 V, I _D = -3.0 A		29.5	39	mΩ
	R _{DS(on)3}	V _{GS} = -2.5 V, I _D = -3.0 A		44	59	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = -10 V, I _D = 1 mA	-0.5	-1.0	-1.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = -10 V, I _D = -3.0 A	5.0	11		S
Drain Leakage Current	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V			-1	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±12 V, V _{DS} = 0 V			±10	μA
Input Capacitance	C _{iSS}	V _{DS} = -10 V		1300		pF
Output Capacitance	C _{oSS}	V _{GS} = 0 V		325		pF
Reverse Transfer Capacitance	C _{rSS}	f = 1 MHz		155		pF
Turn-on Delay Time	t _{d(on)}	I _D = -3.0 A		25		ns
Rise Time	t _r	V _{GS(on)} = -4.5 V		110		ns
Turn-off Delay Time	t _{d(off)}	V _{DD} = -10 V		130		ns
Fall Time	t _f	R _G = 10 Ω		140		ns
Total Gate Charge	Q _G	I _D = -6.0 A		11		nC
Gate to Source Charge	Q _{GS}	V _{DD} = -16 V		2.0		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = -4.5 V		4.0		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 6.0 A, V _{GS} = 0 V		0.8		V
Reverse Recovery Time	t _{rr}	I _F = 6.0 A, V _{GS} = 0 V		60		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		40		nC

TEST CIRCUIT 1 SWITCHING TIME

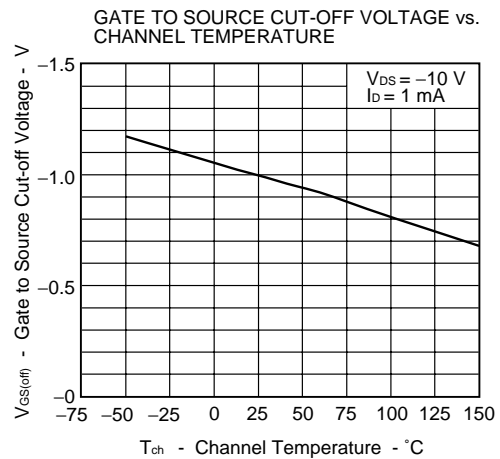
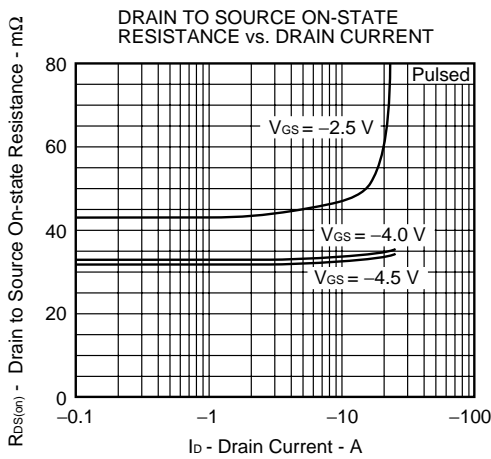
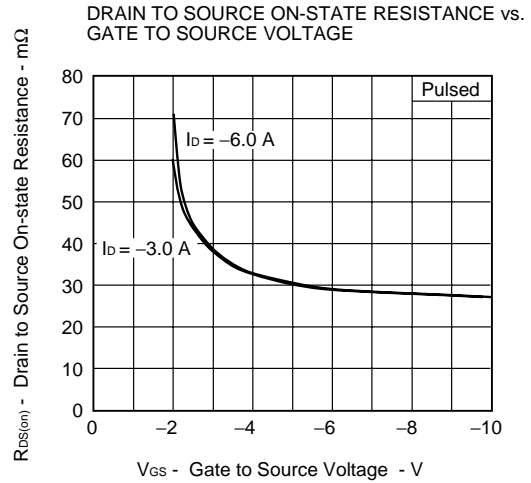
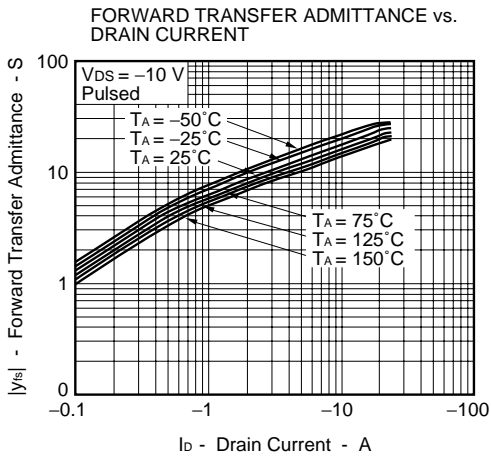
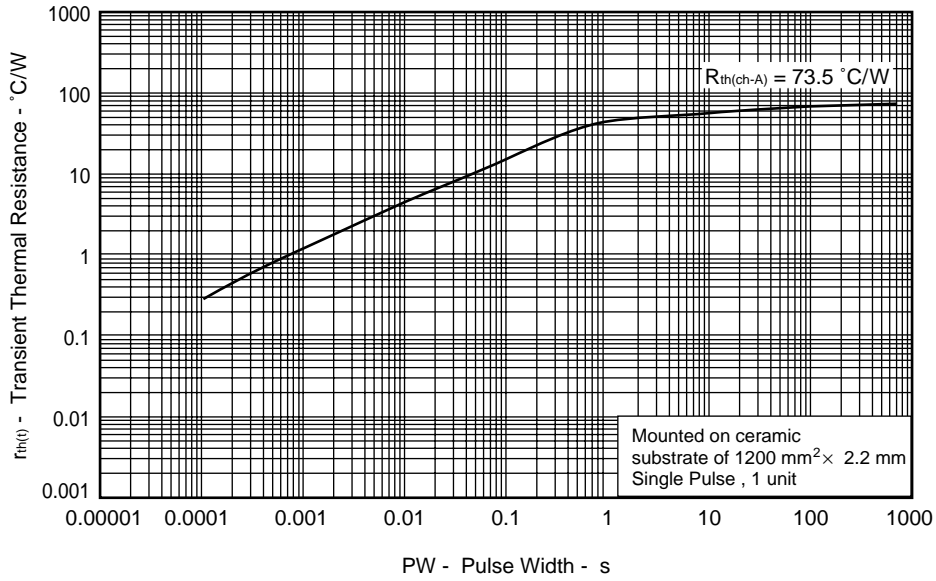


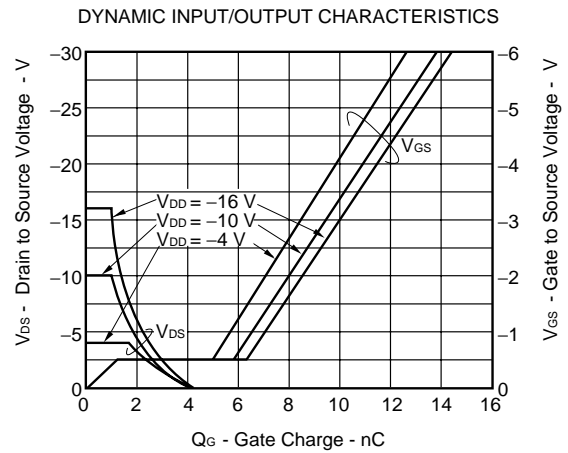
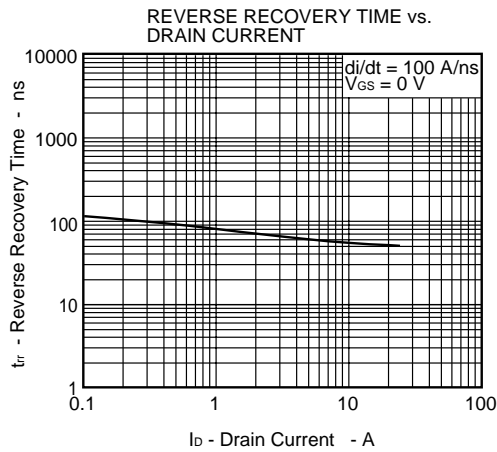
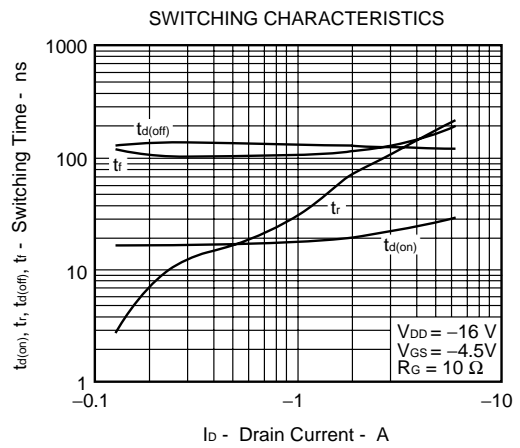
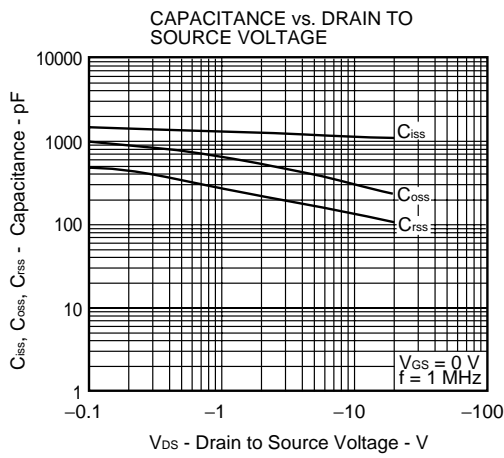
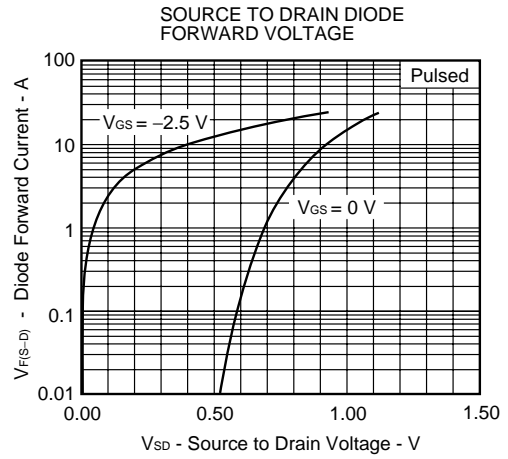
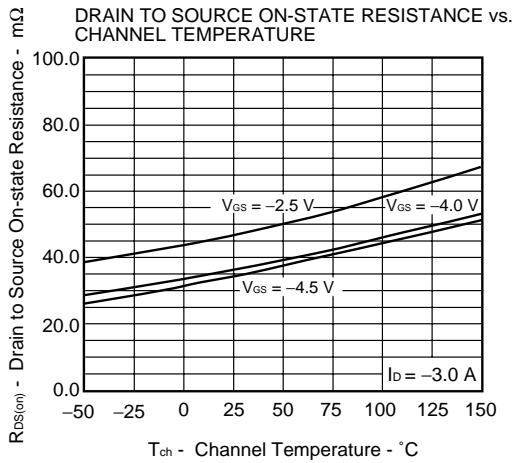
TEST CIRCUIT 2 GATE CHARGE

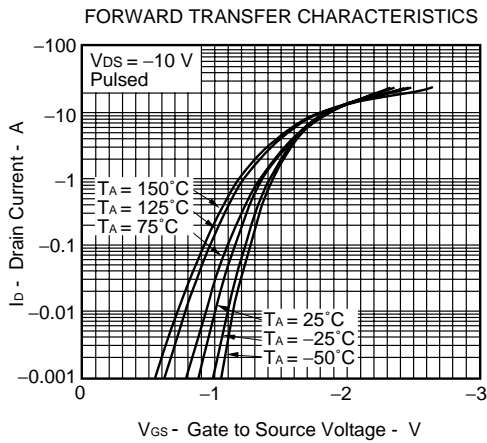
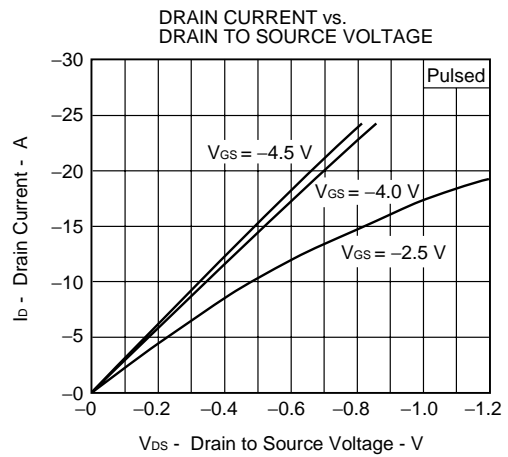
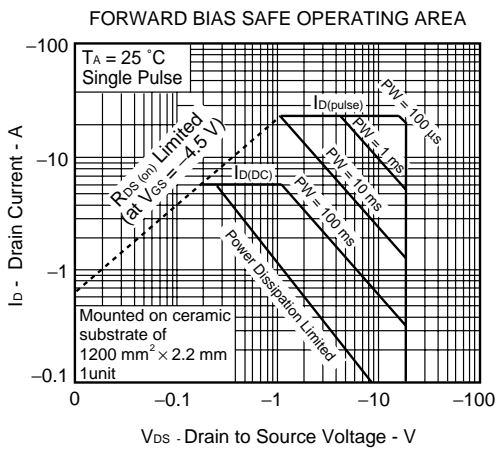
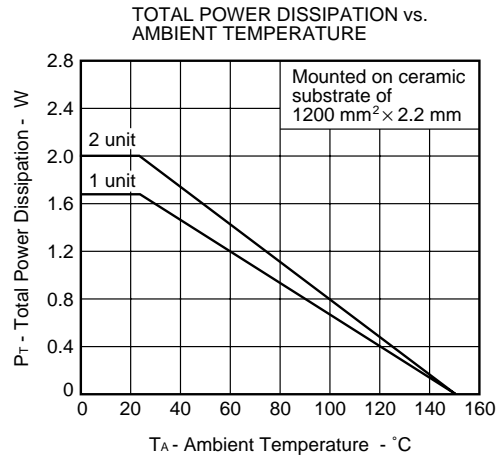
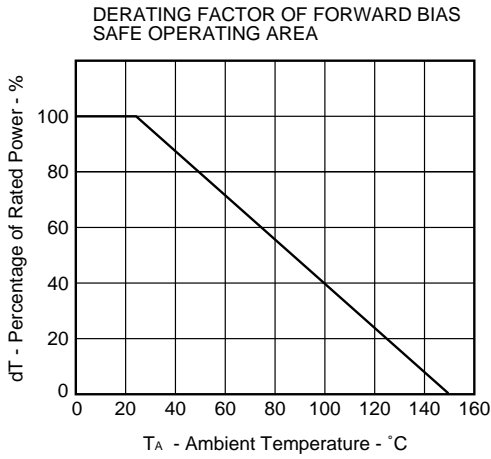


★ TYPICAL CHARACTERISTICS(T_A = 25 °C, All terminals are connected.)

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

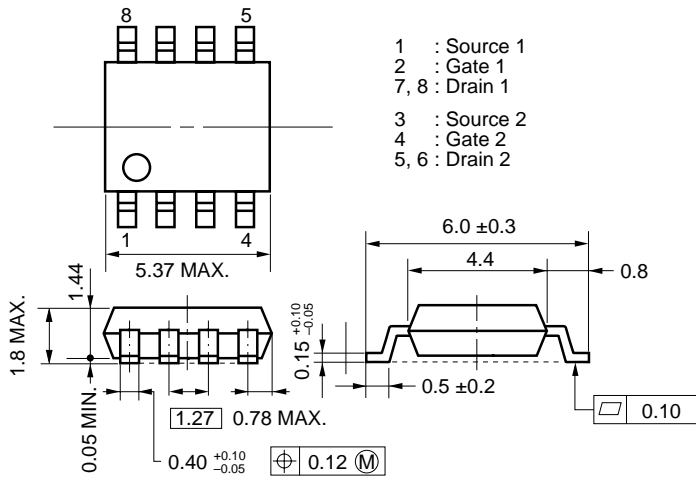






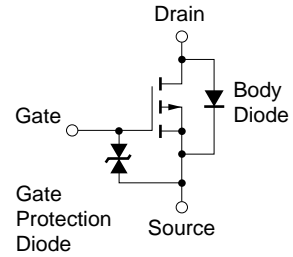
PACKAGE DRAWING (Unit : mm)

Power SOP8



EQUIVALENT CIRCUIT

(1/2 circuit)



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

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